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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,449	07/18/2003	Nobuo Matsui	240541US2DIV	1115

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,449	MATSUI ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/865,289.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/621,449 filed 07/18/2003 and amendment filed 09/27/2005.

2. Claims 1-11 remain pending in the Application.

3. Applicant's arguments have been fully considered, but they are not persuasive.

Specification

4. The disclosure is objected to because of the following informalities:

Page 1 a status of the Application Serial No. 09/865,289 has to be updated.

Page 2 line 14 after "b" insert –e—

Page 2 line 16 after "configurable" insert –e—

Page 4 line 2 after "chang" insert –e--

Page 8 line 20 after "user" delete "specify" insert –specifies--

Appropriate correction is required.

5. Examiner reviewed Applicant's response to this objection. It has to be noted that Examiner has the version of the specification under examination, which received by the office, and this version has typographical errors mentioned above.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1 and 6 recite the limitation "wherein said processor core is designed using **the method** comprising". There is insufficient antecedent basis for this limitation in the claims.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Berekovic et al. *("*A core generator for fully synthesizable and highly parameterizable RISC-cores for system-on-chip designs", Signal Processing Systems, 1998, Pages: 561-568).

With respect to claims 1 and 6 Berekovic et al. teaches a processor as shown on the Fig. 1 which demonstrates a multi-cycle processor core (abstract), a system LSI (abstract) comprising a processor core shown on the Fig. 1; and memory operatively coupled to the processor within connecting the processor shown on the Figure 1 with Inst RAM and Data RAM; wherein the processor is designed using a method comprising: selecting a cache size; selecting an instruction memory size; selecting a data memory size; selecting at least one of a plurality of option instructions to be implemented within the processor by developing a soft core generator for highly parameterizable RISC-cores having an option of the of choosing the instruction word width along with parameters being able configured (abstract), wherein the soft-cores

processors have high flexibility to be configured with arbitrarily chosen parameters by user, such as selecting cache size, selecting a data memory etc. as a fact of inheriting the configuration specifics from the ability of the configuration process of the processors (Pages 562, 563); pages 567-568 also show that selection of cache size (candidates) is selected through parameters, such as data word width.

It has to be noticed that claims 1 and 6 being construed as a product-by-process claims, accordingly product-by-process claims are not limited to the manipulations of the recited steps, only the structure implied by the steps (see MPEP 2113).

With respect to claims 2-5 and 7-9 Berekovic et al. teaches:

claims 2 and 7: the option instructions includes a dividing option instruction (DIV) and a maximum/minimum value option instruction (Page 565);

claims 3 and 8: the processor core is provided with an instructions cache and a data cache as shown on the Fig. 1 with separate instruction RAM (cache) and data RAM (cache) wherein the cache is form of memory in a computer which has a faster access time than most of main memory, and is usually used to store the most frequently accessed data main memory during execution of a program;

claims 4 and 9: the cache size, the option instructions are provided in RTL template within resulting processor cores generated in RTL-HDL (abstract, Page 568);

claim 5: the method further comprises selecting optional hardware associated with the processor within core generator having ability to be used for building block for future system-level synthesis (Conclusion, Page 568).

With respect to claims 10 and 11 Berekovic et al. teaches a method of generating a design of a system LSI using a description language (Title), comprising: preparing a configuration specifying a file including variable item definition information as shown on the Figure 4 wherein the design flow of core processors is depicted and a configuration file is read by a Perl script and flexibility of such method to make changes in the design allows by modifying the instruction set as desired by the designer and using alternative templates files (Page 566); logically composing the design based on the description language model by designing processor cores which are generated in RTL-HDL (Abstract), wherein the variable item definition information contains at least one of option instruction information and information concerning a user defined module and a multiprocessor configuration within flexibility of the design the instruction set can be modified by using all necessary modules as well as the top-level file of the core which are fully synthesizable, wherein an additional instructions can easily added (Page 566); the description language comprises a hardware description language (HDL) (Abstract; Page 563).

Remarks

10. In the remarks Applicant argues in substance:

a) Thereby, in independent claims 1 and 6 a cache memory is selectable from given candidates. Such features are not taught or suggested in Berekovic.

b) claim 10 now further recites "preparing a configuration specifying a file including information concerning a multiprocessor configuration". Such feature as

clarified in independent claim 10 is also believed to be neither taught nor suggested by the applied art to Berekovic.

Examiner respectfully disagrees for the following reasons:

As to a) Berekovic et al. teaches design flow of the cores depicted on the Figure 4, wherein a perl script reads a **configuration file (from given candidates)** to generate a structural VHDL description of the core (page 566), wherein the soft-core approach offers **high flexibility** for the selection of implementation parameters (page 568). Pages 567-568 also show that selection of cache size (candidates) is selected through parameters, such as data word width.

As to b) Berekovic et al. teaches the soft-core approach offers **high flexibility** for the selection of implementation parameters, wherein data and instruction word width of the cores can be changed independently of each other, enabling the designer to fully explore the design in terms of computational speed, silicon area and flexibility (page 568). Moreover as shown in the table 1 of the page 567, wherein the results of the synthesis for **different processor types** are depicted (page 567).

Based on at least these disclosures in Berekovic et al. the rejection under 35 USC § 102 is maintained.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

STACY A. WHITMORE
PRIMARY EXAMINER

Examiner
Helen Rossoshek
AU 2825